

GR 99 P 1878 - Application No. 09/590,041  
Response to Office action 4/11/2006  
Response submitted July 11, 2006

### Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

### Listing of Claims:

Claim 1 (currently amended). A power switch, comprising:

a controllable transistor having a load path and a control electrode;

a first limiting transistor for limiting a voltage drop across said load path of said first transistor, said first limiting transistor having a load path connected in series with said load path of said ~~first~~ controllable transistor, and having a control electrode; and

at least one second limiting transistor having a load path connected in series with said load path of said first limiting transistor;

~~an~~ a first auxiliary transistor having a load path connected between said control electrode of said first limiting transistor and a reference node, and having a control electrode connected between said ~~first~~ controllable transistor and said first limiting transistor;

at least one second auxiliary transistor having a load path connected between said control electrode of said first limiting transistor and said control electrode of said second limiting transistor; and

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a control electrode connected between said load paths of said first and second limiting transistors.

Claim 2 (canceled).

Claim 3 (currently amended). The power switch according to claim 1, wherein said load path of said ~~controlled~~ controllable transistor is connected between said limiting transistor and said reference node.

Claim 4 (original). The power switch according to claim 1, which further comprises a power switch control terminal connected to said control electrode of said controllable transistor.

Claim 5 (canceled).

Claim 6 (currently amended). The power switch according to ~~claim 2, wherein claim~~ 1, wherein each of said first and at least one second limiting transistors has a source electrode and a gate electrode, and a Zener diode is connected between said source electrode and said gate electrode of each said limiting transistor.

Claim 7 (canceled).

Claim 8 (currently amended). The power switch according to ~~claim 2, which claim 1,~~ which comprises Zener diodes connected in parallel with said load paths of each said auxiliary transistor.

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Claim 9 (canceled).

Claim 10 (currently amended). The power switch according to ~~claim 2, wherein~~  
claim 1, wherein said controllable transistor is a MOSFET of a first conductivity type,  
said first and second limiting transistors are normally on field-effect transistors of the  
first conductivity type, and said first and second auxiliary transistors are normally on  
field-effect transistors of a second conductivity type.

Claim 11 (canceled).

Claim 12 (original). The power switch according to claim 1, wherein said controllable  
transistor, said first and second limiting transistors, and said first and second  
auxiliary transistors are integrated in a semiconductor body.

Claim 13 (withdrawn - currently amended). A semiconductor configuration,  
comprising:

a semiconductor body and a power switch formed in said semiconductor body and  
having a load path running vertically through said semiconductor body;

~~said a~~ a semiconductor body ~~being~~ formed with:

a substrate doped with charge carriers of a first conductivity type;

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at least one well doped with charge carriers of a second conductivity type, and  
a MOSFET formed in said at least one well;

a first region formed in said substrate spaced apart from said well and heavily  
doped with charge carriers of the first conductivity type; and

a second region horizontally spaced apart from said first region and heavily  
doped with charge carriers of a second conductivity type; and

a power switch according to claim 1 formed in said semiconductor body and having a  
load path running vertically through said semiconductor body.

Claim 14 (withdrawn). The semiconductor body according to claim 13, wherein said  
first region is one of a plurality of first regions formed in said semiconductor body and  
spaced apart from one another in the vertical direction, and said second region is  
one of a plurality of second regions formed in said semiconductor body and spaced  
apart from one another in the vertical direction.

Claim 15 (withdrawn). The semiconductor body according to claim 14, which  
comprises interconnects connecting respectively adjacent second regions, said  
interconnects being formed by doping with charge carriers of the second conductivity  
type, and wherein said well is connected to one of said second regions by an  
interconnect.